CLAIMS

1. A memory structure comprising:

a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region;

a gate layer formed over said channel region of said substrate;

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays to pass through said tunable interlayer dielectric to said gate layer.

2. The memory structure of claim 1, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

3. The memory structure of claim 2, wherein said corresponding crystal director has a random orientation within said matrix during said opaque state.

4. The memory structure of claim 3, wherein said opaque state is enabled when an electric field is not applied across said tunable interlayer dielectric.

5 The memory structure of claim 3, wherein said opaque state is enabled when a magnetic field is applied across said tunable interlayer dielectric.

6. The memory structure of claim 2, wherein said corresponding crystal director has a uniform orientation within said matrix during said transparent state.

7. The memory structure of claim 6, wherein said transparent state is enabled when an electric field is applied across said tunable interlayer dielectric.

8. The memory structure of claim 6, wherein said transparent state is enabled when a magnetic field is not applied across said tunable interlayer dielectric.

9. The memory structure of claim 1, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

10. The memory structure of claim 1, wherein said matrix is polymer.

11. The memory structure of claim 1, wherein said gate layer includes a charge storing layer

12. A method for fabricating a memory structure, said method comprising:

depositing a tunable interlayer dielectric over a wafer, said wafer including a substrate and a gate layer, said gate layer including a charge storing layer, said tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays from passing through said tunable interlayer dielectric to said gate layer.

13. The method of claim 12, further comprising generating an electric field across said tunable interlayer dielectric to switch said tunable interlayer dielectric to said transparent state.

14. The method of claim 13, further comprising exposing said gate layer to UV rays through said tunable interlayer dielectric.

15. The method of claim 14, further comprising terminating said electric field across said tunable interlayer dielectric.

16. The method of claim 12, further comprising not generating a magnetic field across said tunable interlayer dielectric to switch said tunable interlayer dielectric to said transparent state.

17. The method of claim 16, further comprising exposing said gate layer to UV rays through said tunable interlayer dielectric.

18. The method of claim 17, further comprising generating said magnetic field across said tunable interlayer dielectric.

19. The method of claim 12, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

20. The method of claim 12, wherein said matrix is polymer.

21. The method of claim 12, wherein said gate layer includes a charge storing layer.

22. A memory structure comprising a substrate having a drain region, a source region and a channel region, said channel region being between said source region and said drain region, said memory structure further comprising a gate layer formed over said channel region of said substrate, said gate layer including a charge storing layer, said memory structure characterized by:

a tunable interlayer dielectric formed over said gate layer and said substrate, said tunable interlayer dielectric comprising a matrix and tunable material situated within said matrix, said tunable interlayer dielectric having a transparent state and an

opaque state, said transparent state allowing UV rays to pass through said tunable interlayer dielectric to said gate layer, said opaque state preventing UV rays from passing through said tunable interlayer dielectric to said gate layer.

23. The memory structure of claim 22, wherein said tunable material comprises a plurality of liquid crystal droplets, each of said plurality of liquid crystal droplets having a corresponding crystal director, said corresponding crystal director defining a polar orientation of each of said plurality of liquid crystal droplets.

24. The memory structure of claim 23, wherein, during said opaque state, said corresponding crystal director has a random orientation within said matrix.

25. The memory structure of claim 23, wherein, during said transparent state, said corresponding crystal director has a uniform orientation within said matrix.

26. The memory structure of claim 25, wherein said transparent state is enabled by providing an electric field through said tunable interlayer dielectric.

27. The memory structure of claim 22, wherein said tunable material is selected from the group consisting of electrically tunable material and magnetically tunable material.

28. The memory structure of claim 22, wherein said matrix is polymer.

29. The memory structure of claim 22, wherein said gate layer includes a charge storing layer.